IN THE CLAIMS:

Please cancel claims 2, 9, and 15 without prejudice, and amend the claims as follows:

1. (Currently Amended) A memory apparatus, comprising:

at least one cell array having a plurality of memory cells, each memory cell having an associated word line and an associated bit line;

a control device having a signaling connection to a plurality of word lines and bit lines wherein the control device is configured to:

execute a destructive read command for reading data from at least one memory cell, the destructive read command comprising:

electrically biasing a bit line associated with the at least one memory cell;

~~opening~~ after electrically biasing, activating a word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line; and

destructively reading data stored in the at least one memory cell, whereby the read data is destroyed as a result of reading the data; and

execute a destructive write command for writing data to the at least one memory cell, the destructive write command comprising:

writing data to the at least one memory cell without first reading stored data in the memory cell.

2. (Cancelled) ~~The memory apparatus of claim 1, wherein the control device is further configured to execute a write command for writing data to at least one memory cell, the write command comprising:~~

~~writing data to the at least one memory cell without first reading stored data in the memory cell.~~

3. (Currently Amended) The memory apparatus of claim 1, wherein the control device is further configured to execute a nondestructive read command for reading data from at least one of the memory cells, the nondestructive read command comprising:

electrically biasing the bit line associated with the at least one memory cell;

~~opening~~ after electrically biasing, activating the word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line;

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

4. (Currently Amended) The memory apparatus of claim 1, wherein the control device is further configured to execute a refresh command for refreshing data stored in at least one memory cell, the refresh command comprising:

electrically biasing the bit line associated with the at least one memory cell;

~~opening~~ after electrically biasing, activating the word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line;

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

5. (Original) The memory apparatus of claim 1, wherein the memory apparatus is a DRAM.

6. (Original) The memory apparatus of claim 1, wherein the memory apparatus is an SRAM.

7. (Original) The memory apparatus of claim 1, wherein the memory apparatus is a buffer storage device.

8. (Currently Amended) A method for operating a plurality of memory cells in a memory apparatus, the method comprising:

executing a destructive read command for reading data from at least one memory cell, the destructive read command, comprising:

electrically biasing [[the]] a bit line associated with the at least one memory cell;

~~opening~~ after electrically biasing, activating [[the]] a word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line; and

destructively reading data stored in the at least one memory cell, whereby the read data is destroyed as a result of reading the data; and

executing a destructive write command for writing data to the at least one memory cell, the destructive write command comprising:

writing the data to the at least one memory cell without first reading stored data in the memory cell.

9. (Cancelled) ~~The method of claim 8, further comprising:~~

~~executing a destructive write command for writing data from at least one memory cell, the destructive write command comprising:~~

~~writing the data to the at least one memory cell without first reading stored data in the memory cell.~~

10. (Currently Amended) The method of claim [[9]] 8, further comprising:

executing a nondestructive read command for reading data from at least one memory cell, the nondestructive read command comprising:

electrically biasing the bit line associated with the at least one memory cell;

~~opening~~ activating the word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line; and

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

11. (Currently Amended) The method of claim 10, further comprising:

executing a refresh command for refreshing data in at least one memory cell, the refresh command comprising:

electrically biasing the bit line associated with the at least one memory cell;

~~opening~~ activating the word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line; and

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

12. (Currently Amended) The method of claim 8, further comprising:

executing a nondestructive read command for reading data from at least one memory cell, the nondestructive read command comprising:

electrically biasing the bit line associated with the at least one memory cell;

~~opening~~ activating the word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line; and

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

13. (Currently Amended) The method of claim 8, further comprising:

executing a refresh command for refreshing data in at least one memory cell, the refresh command comprising:

electrically biasing the bit line associated with the at least one memory cell;

~~opening~~ activating the word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line; ~~and~~

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

14. (Currently Amended) A memory apparatus, comprising:

at least one cell array having a plurality of memory cells having associated word lines and associated bit lines;

a control means for:

executing a destructive read command for reading data from at least one memory cell, the destructive read command comprising:

electrically biasing a bit line associated with the at least one memory cell;

~~opening~~ after electrically biasing, activating a word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line; and

destructively reading data stored in the at least one memory cell, whereby the read data is destroyed as a result of reading the data; and

executing a destructive write command for writing data to the at least one memory cell, the destructive write command comprising:

writing data to the at least one memory cell without first reading stored data in the memory cell.

15. (Cancelled) ~~The memory apparatus of claim 14, wherein the control means is further configured for executing a write command for writing data to at least one memory cell, the write command comprising:~~

~~writing data to the at least one memory cell without first reading stored data in the memory cell.~~

16. (Currently Amended) The memory apparatus of claim [[15]] 14, wherein the control means is further configured for executing a nondestructive read command for reading data from at least one of the memory cells, the nondestructive read command comprising:

electrically biasing the bit line associated with the at least one memory cell;

~~opening~~ activating the word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line;

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

17. (Currently Amended) The memory apparatus of claim 16, wherein the control means is further configured for executing a refresh command for refreshing data stored in at least one memory cell, the refresh command comprising:

electrically biasing the bit line associated with the at least one memory cell;

~~opening~~ activating the word line associated with the at least one memory cell, thereby connecting the at least one memory cell to the bit line;

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

18. (Original) The memory apparatus of claim 17, wherein the memory apparatus is a DRAM.

19. (Original) The memory apparatus of claim 17, wherein the memory apparatus is an SRAM.

20. (Original) The memory apparatus of claim 17, wherein the memory apparatus is a buffer storage device.